EVENT STRUCTURES AND REFINEMENT FOR RELAXED MEMORY

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OVERVIEW

Context
Event structures
Thin air reads
Synchronization actions
Program refinement
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CONTEXT

import usual.chit.chat.JMM;
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State of the art:

- Formal models of valid executions: JMM, C11, ARM/POWER, x86-TSO, ... (Mile high view: partially ordered events labelled with R/W actions)
- DRF theorem.
- Lots of lovely tooling (mechanized models, theorems, test cases, ...)

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- Compiler optimizations not validated against model.
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Can we use existing models of relaxed concurrency?
EVENT STRUCTURES

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- A partial order $(E, \leq)$ (events with program order)
- A function $\lambda : E \rightarrow \Sigma$ (labelling)
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- A function $\lambda : E \to \Sigma$ (labelling)
- A binary relation $\#$ on $E$ (conflict)
- If $d \# e$ then $d \neq e$, and if $c \# d \leq e$ then $c \# e$
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For example the event structure for $r=x; \ y=r$ is:

![Diagram of event structure]

$R_x = 0 \quad \text{init} \quad R_x = 1$

$W_y = 0 \quad W_y = 1$
EVENT STRUCTURES

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- First configuration is fine, but second is fishy, where did $x = 1$ come from?
- Assume relations $\text{RWJ}$ and $\text{RWC}$ on $\mathcal{E}$.
- (E.g. $\text{RWC}$ is r/w same location, $\text{RWJ}$ is r/w same location+value).
- Write $d^2 \text{RWC}(e)$ for $d^2 \mathcal{RWC}(e)$:
  - $(d = e)$ and $(d \# e)$.
  - Ditto $\text{RWJ}$.
- Define $d$ is a **justifier** for $e$ when $e \neq d$, $d^2 \text{RWJ}(e)$, and there is no $c$ where $c^2 \text{RWC}(e)$.
- A configuration is **justified** if all non-initial events have a justifier.
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![Diagram](image)

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Write $d \in \text{RWC}(e)$ for $\lambda(d) \in \text{RWC}(\lambda(e))$, $\neg(d = e)$ and $\neg(d \# e)$. Ditto RWJ.
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A configuration is **totally ordered** when there is a total order $\leq_{to}$ such that $d \leq e$ implies $d \leq_{to} e$.

Define $d$ is a **sequential justifier** for $e$ when $d \leq_{to} e$, $d \in RWJ(e)$, and there is no $d \leq_{to} c \leq_{to} e$ where $c \in RWC(e)$.

A configuration is **sequentially consistent** if it can be totally ordered such that all non-initial events have a sequential justifier.
EVENT STRUCTURES

An IRIW example:

thread 1: \( x=1; \)
thread 2: \( y=1; \)
thread 3: \( r=x; \text{ if}(r) \ r=y; \)
thread 4: \( r=y; \text{ if}(r) \ r=x; \)
EVENT STRUCTURES

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- thread 1: \( x=1; \)
- thread 2: \( y=1; \)
- thread 3: \( r=x; \) if\((r)\) \( r=y; \)
- thread 4: \( r=y; \) if\((r)\) \( r=x; \)

Has justified non-SC configuration:
EVENT STRUCTURES

The basic model is event structures with justified configurations.

Elegant model with pretty pictures (thanks Glynn!).
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Basic model doesn't do everything:

- Thin Air Reads.
- Synchronization actions (volatile fields, locks, ...).
- Refinement relation to validate compiler optimizations.
Oh dear, the TAR pit:

thread 1: \( r = x; \ y = r \);
thread 2: \( r = y; \ x = r \);
Oh dear, the TAR pit:

thread 1: r=x; y=r;
thread 2: r=y; x=r;

Has justified configuration:

A TAR caused by a cycle in (justification + program-order).
Banning such cycles kills instruction reordering:

thread 1: \( r=x;\ y=1; \)
thread 2: \( r=y;\ x=1; \)

since the expected behaviour has exactly the same cycle:
**THIN AIR READS**

**Handwave**: allow conflict when avoiding TAR.

Analogous to JMM candidate executions.

---

**A configuration** is a downclosed, #-free set of events.

**A pre-configuration** is a downclosed set of events.

A pre-configuration is relaxed justified when it has a total order such that any non-initial \(e\) has a justifier \(j(e)\) to \(e\).

A configuration is relaxed justified when it is included in a relaxed justified pre-configuration.

Proposal: allowed executions are relaxed justified configurations.

**DRF Theorem** holds for relaxed justified configurations (under some mild technical conditions).
**Handwave**: allow conflict when avoiding TAR.

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THIN AIR READS

The stuff I just brushed under the carpet...

Properties of the alphabet:
- If $a \in \text{RWC}(b)$ and $b \in \text{RWC}(c)$ then $a \in \text{RWC}(c)$.

Properties of the event structure:
- If $c < d \sim e$ then $c \leq e$.
- If $c \# d \sim e$ and $c \not\geq e$ then $c \# e$.
- If $d \sim e$ and $\lambda(d) \in \text{RWC}(a)$ then $\lambda(e) \in \text{RWC}(a)$.
- If $d \sim e$ and $a \in \text{RWC}(\lambda(d))$ then $a \in \text{RWC}(\lambda(e))$.
- If $d \sim e$ and $a \in \text{RWJ}(\lambda(d))$ then $a \not\in \text{RWJ}(\lambda(e))$.
- For any $a \in \text{RWC}(\lambda(e))$ there is a $d \sim e$ where $a \in \text{RWJ}(\lambda(d))$.

where $d \sim e$ is the minimal conflict relation:
- $d \sim e$ whenever $d \# e$ and if $d \geq b \# c \leq e$ then $d = b \# c = e$.

In example programs, $d \sim e$ is generated by conflicting reads.
THIN AIR READS

Instruction reordering example:

thread 1: \( r=x; \ y=1; \)
thread 2: \( r=y; \ x=1; \)

includes relaxed justified configuration:
Speculative read example:

thread 1: \( r = x; \) if \( r \) \( y = 1; \)
thread 2: \( r = y; \) \( x = 1; \)

includes relaxed justified configuration:
Another TAR pit:

thread 1:  \( r=x; \) if(\( r \)) y=1;
thread 2:  \( r=y; \) if(\( r \)) x=1;

is cyclic, so this configuration is not relaxed justified:
SYNCHRONIZATION ACTIONS

Model so far is only for relaxed memory.
Let's add synchronization actions (motivating example: Java volatiles).
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Let's add synchronization actions (motivating example: Java volatiles).
Assume \( \text{Sync} \subseteq \Sigma \).

In a totally ordered configuration, this introduces **synchronization** relation:

\[
\lambda(d), \lambda(e) \in \text{Sync} \quad d \leq_{to} e \quad \lambda(d) \in \text{RWC}(\lambda(e))
\]

\[
d \leq_{so} e
\]

and **happens before** order:

\[
\begin{align*}
& d \leq e & & d \leq_{so} e & & c \leq_{hb} d \leq_{hb} e \\
& d \leq_{hb} e & & d \leq_{hb} e & & c \leq_{hb} e
\end{align*}
\]

(Note that if there are no synchronization actions then \( \leq \) is the same as \( \leq_{hb} \)).
SYNCHRONIZATION ACTIONS

Recall that in the absence of synchronization actions, 
\( d \) is a justifier for \( e \) when \( e \not\preceq d, \ d \in \text{RWJ}(e) \), and 
there is no \( d \leq c \leq e \) where \( c \in \text{RWC}(e) \).
SYNCHRONIZATION ACTIONS

In the presence of synchronization actions, 

\( d \) is a justifier for \( e \) when \( e \not\preceq_{hb} d, \ d \in \text{RWJ}(e), \) and 

there is no \( d \preceq_{hb} c \preceq_{hb} e \) where \( c \in \text{RWC}(e). \)
SYNCHRONIZATION ACTIONS

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(These definitions coincide when there are no synchronization actions.)
SYNCHRONIZATION ACTIONS

In the presence of synchronization actions, $d$ is a justifier for $e$ when $e \not\leq_{hb} d$, $d \in RWJ(e)$, and there is no $d \leq_{hb} c \leq_{hb} e$ where $c \in RWC(e)$.

(These definitions coincide when there are no synchronization actions.) Previous definitions and results go through, under some more technical requirements...
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- If \( a \in RWC(b) \) and \( a \in \text{Sync} \) then \( b \in \text{Sync} \) (this fails in C11)
- If \( d \sim e \) and \( d \in \text{Sync} \) then \( e \in \text{Sync} \).

in a relaxed justified pre-configuration:

- If \( e \) is a synchronization event, then \( j(e) \) sequentially justifies \( e \).
- If \( d \leq_{hb} j(e) \) then \( \neg (d \# e) \).

and in a relaxed justified configuration \( C \):

- If \( j(e) \leq_{hb} j(e) \) and \( e \in C \) then \( j(e) \in C \).
SYNCHRONIZATION ACTIONS

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in a relaxed justified pre-configuration:

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- If \( d \leq_{hb} j(e) \) then \( \neg(d \neq e) \).

and in a relaxed justified configuration \( C \):

- If \( j(e) \leq_{hb} c \leq_{hb} e \) and \( e \in C \) then \( j(e) \in C \).

**DRF Theorem** still holds.
PROGRAM REFINEMENT

Looking for a definition of refinement $\sqsubseteq$ between event structures which is:

- is a preorder
- is compositional: if $P \sqsubseteq Q$ then $C[P] \sqsubseteq C[Q]$ for any program context $C$
- validates common compiler optimizations (roach motel, variable reordering and thread inlining)
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We have one.
PROGRAM REFINEMENT

Define $ES_1 \subseteq ES_2$ whenever

- there is a binary relation $R \subseteq E_1 \times E_2$,
- for every $e_2 \in E_2$ there is $e_1 \in E_1$ such that $(e_1, e_2) \in R$,
- for every $(e_1, e_2) \in R$, we have $\lambda_1(e_1) = \lambda_2(e_2)$,
- for every $(d_1, d_2) \in R$ and $(e_1, e_2) \in R$, we have $d_1 \not\#_1 e_1$ iff $d_2 \not\#_2 e_2$,
- for every synchronized write $d_2$ with $(d_1, d_2) \in R$ and $d_2 \lt_2 e_2$, there exists $d_1 \lt_1 e_1$ such that $(e_1, e_2) \in R$,
- for every synchronized read $e_2$ with $(e_1, e_2) \in R$ and $d_2 \lt_2 e_2$, there exists $d_1 \lt_1 e_1$ such that $(d_1, d_2) \in R$, and
- for every synchronized read $e_2$ with $(e_1, e_2) \in R$ and $d_2 \ll_2 e_2$, there exists $d_1 \ll_1 e_1$ such that $(d_1, d_2) \in R$.

where $d \ll e$ whenever $d < c < e$ for some $c \in WWC(d)$. 
PROGRAM REFINEMENT

\( \sqsubseteq \) is a preorder.

\( E_1 \sqsubseteq E_2 \) whenever:

\[ E_1 = E_2 \]

\[ 1 \#_1 = 2 \]

\[ 1 = 2 \]

that is, more things are related by program order in \( ES_2 \) than in \( ES_1 \).
PROGRAM REFINEMENT

□ is a preorder.

□ is compositional, in that it respects the following operations:
  • Prefixing (\(a.ES\) adds a new event labelled \(a\) to the beginning of \(ES\)).
  • Parallel composition (\(ES_1 | ES_2\) is the disjoint union of \(ES_1\) and \(ES_2\)).
  • Sum (\(ES_1 + ES_2\) is \(ES_1 | ES_2\), but with conflict between \(E_1\) and \(E_2\)).

Enough to give semantics for a simple shared-memory concurrent language.
PROGRAM REFINEMENT

⊑ is a preorder.
⊑ is compositional.
⊑ validates roach motel and variable reordering, since $a. b. ES \sqsubseteq b. a. ES$ whenever:

- $a \not\in WWC(b)$,
- $a$ is not a synchronized read, and
- $b$ is not a synchronized write.
PROGRAM REFINEMENT

⊑ is a preorder.
⊑ is compositional.
⊑ validates roach motel and variable reordering.
⊑ validates thread inlining, since $ES_1 \sqsubseteq ES_2$ whenever:

$$E_1 = E_2 \quad \leq_1 \subseteq \leq_2 \quad \#_1 = \#_2 \quad \lambda_1 = \lambda_2$$

that is, more things are related by program order in $ES_2$ than in $ES_1$. 
TO DO LIST

Tooling.

Conjecture: program refinement respects relaxed justified configurations.

Per-location SC (aka coherence).

Richer alphabets of synchronization actions.

Object creation (c.f. Lochlieber).

Reasoning by invariants (e.g. type safety).

Specification language for APIs to describe synchronization (currently done by English, e.g. in java collections API).
CONCLUSIONS

Event structures provide a model for relaxed memory.

Basic model is event structures with justified configurations.

Scales up (at cost of complexity) to TAR and synchronization actions.

Supports program refinement which handles common optimizations (roach motel, variable reordering and thread inlining).